Session 19 Overview

Analog Techniques

Chair: Axel Thomsen, Silicon Laboratories, Austin, TX

Associate Chair: Doug Smith, SMSC, Austin, TX

The field of analog circuit design always yields a wide variety of interesting applications, tricks, and techniques. The papers in this session predominantly deal with the classic challenges of power efficiency and compensation of complex feedback circuits.

The first 3 papers address the area of high-power audio amplifiers. There is a continued drive to achieve higher output power at high efficiency and high level of integration with acceptable levels of distortion. The first paper, 19.1 is a class-D amplifier that offers an output power of 240W. In this open-loop design, the key is the design of the gate drive. Paper 19.2 addresses the unique challenges of compensation of a linear audio amplifier due to the presence of a large gate capacitance of the output device. Paper 19.3 presents a class-D amplifier with digital input that utilizes a closed-loop architecture for improved distortion. While the power stage is external, the controller has to be designed to guarantee stability.

The next 3 papers highlight a variety of interesting details in such classic analog circuit blocks as regulators, filters, and opamps. Paper 19.4 has been withdrawn. Paper 19.5 offers an interesting simple design for a continuous-time filter. Here the linearity and overdrive voltage of the devices are linked in an unusual manner allowing for a low-power optimization. Paper 19.6 advances the state-of-the-art in the area of chopper stabilized amplifiers. It introduces a notch filter in the signal path that removes the ripple commonly produced by the upmodulation of the chopping artifacts.

The final 2 papers come from the area of switching power supplies. Paper 19.7 shows a benchmark paper for a completely integrated switching power supply. To achieve a competitive power efficiency, extra-thick top-level copper is used and a variety of design techniques applied to enable the elimination of all external devices. Paper 19.8 presents a technique for a boost converter. It aims to eliminate the loss of a diode voltage by replacing it with a driven MOS switch. The circuit achieves a turn-on time of 20ns.

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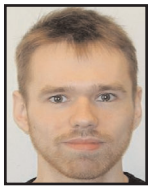

19.1 A 240W Monolithic Class-D Audio Amplifier Output Stage **1:30 PM**

F. Nyboe, Texas Instruments, Lyngby, Denmark and Ørsted*DTU, Lyngby, Denmark

A single-channel class-D audio amplifier output stage outputs 240W unclipped into 4Ω. 0.1% open-loop THD+N allows using the device in a fully-digital audio signal path with no feedback. The output current capability is ±18A and the part is fabricated in a 0.4µm/1.8µm high-voltage BiCMOS process. Over-current sensing protects the output from short circuits.

19.2 Frequency Compensation of an SOI Bipolar-CMOS-DMOS Car Audio PA **2:00 PM**

R. van der Zee, University of Twente, Enschede, The Netherlands

A car audio PA uses a frequency-compensation scheme that avoids large compensation capacitors while retaining the bandwidth and stable load range of nested Miller compensation. The THD is 0.005% at 1kHz and 10W output power. The SNR is 108dB and the amplifier is stable for any passive load up to 50nF. The PA is fabricated in a 1µm SOI bipolar-CMOS-DMOS process.

19.3 A Digital Input Controller for Audio Class-D Amplifiers with 100W 0.004% THD+N and 113dB DR **2:30 PM**

T. Ido, Texas Instruments, Kanagawa, Japan

A digital input controller for audio class-D amplifiers is presented. The controller utilizes specially configured integrated DAC and power stage feedback loop to suppress distortion components coming from power-stage switching with digital input capability. The class-D amplifier system with the controller and an existing power stage achieves 113dB DR, 0.0018% THD+N with 10W output power, and 0.004% THD+N with 100W output power into 4Ω load.

19.4 Paper Withdrawn

19.5 A 4.1mW 79dB DR 4th-order Source-Follower-Based Continuous-Time Filter for WLAN Receivers **3:15 PM**

S. D'Amico, University of Lecce, Lecce, Italy

Using a composite source-follower with positive feedback to synthesize complex poles, a single-branch CMOS biquad achieves large linearity at low overdrive voltage, saving power. In 0.18µm CMOS with a 1.8V supply, a 4th-order 10MHz filter for WLAN applications achieves 17.5dBm IIP3 and -40dB HD3 for a 600mV$_{pp_diff}$ input signal amplitude. A 24µV$_{rms}$ noise gives a 79dB DR while drawing 2.25mA from 1.8V.

19.6 A Micropower Chopper-Stabilized Operational Amplifier Using an SC Notch Filter with Synchronous Integration Inside the CT Signal Path **3:45 PM**

R. Burt, Texas Instruments, Tucson, AZ

A micropower chopper-stabilized opamp uses an SC notch filter with synchronous integration inside the CT signal path to eliminate chopping noise. Characteristics include rail-to-rail I/O, 15µA supply current at 1.8 to 5.5V, 2µV offset, 55nV/√Hz noise, 350kHz GBW, and a chopping frequency of 125kHz. The Die area is 0.7mm^2 using 0.6µm CMOS.

19.7 A Multi-Stage Interleaved Synchronous Buck Converter with Integrated Output Filter in a 0.18µm SiGe Process

S. Abedinpour, Freescale Semiconductor, Tempe, AZ **4:15 PM**

A fully integrated 0.18µm SiGe synchronous buck DC/DC converter with an on-chip LC output filter supporting a maximum output current of 200mA and efficiency of 64% is presented. The converter utilizes a 10µm-thick electroplated copper layer for integrated inductors and gate capacitors. High switching frequency of 45MHz, multi-phase interleaved operation, and fast hysteretic control reduces the filter inductor and capacitor sizes by two orders of magnitude enabling a fully integrated converter.

19.8 A CMOS-Control Rectifier for Discontinuous-Conduction Mode Switching DC-DC Converters **4:45 PM**

T. Man, Hong Kong University of Science and Technology, Hong Kong, China

A sub-1V boost converter with a CMOS-control rectifier enables adaptive dead-time control and mV-range forward-voltage drop. This converter can operate with <0.9V input and deliver 2.5V and 250mW output with 85% efficiency and is intended for single-cell battery-powered mobile systems.